

ABSTRACT OF THE DISCLOSURE

A non-volatile semiconductor memory comprises a memory cell array having a plurality of non-volatile memory cells, at least one reference cell, a read circuit for reading data by applying a first voltage to one of word lines to compare a current flowing through one of bit lines with a current flowing through the reference cell, an erase circuit for erasing the data by applying a voltage to at least two selected from the word lines, the bit lines, the source lines and a semiconductor region including the memory cells, first and second regulators, and an erase verify circuit for detecting whether the erase has finished by applying an output voltage of the first regulator to word lines of the memory cells to be erased, while applying an output voltage of the second regulator to a word line of the reference cell, thereby comparing a cell current of selected one of the memory cells with a cell current of the reference cell.